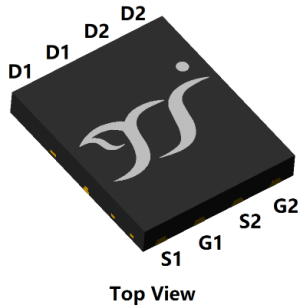
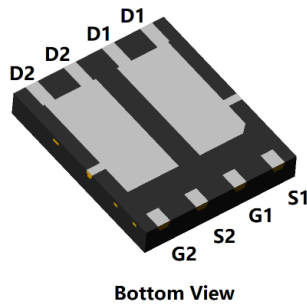


N-Channel and P-Channel Complementary MOSFET

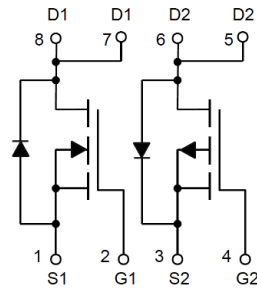


Top View



Bottom View

DFN5060-8L



Product Summary

NMOS

- V_{DS} 100V
- I_D 10A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 110 m Ω
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 120 m Ω

PMOS

- V_{DS} -100V
- I_D -18A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) < 110 m Ω
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) < 120 m Ω
- 100% EAS Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

| Parameter | | Symbol | NMOS | PMOS | Unit |
|--|-------------------|----------------|----------|----------|------------|
| Drain-source Voltage | | V_{DS} | 100 | -100 | V |
| Gate-source Voltage | | V_{GS} | ± 20 | ± 20 | V |
| Drain Current | $T_A=25^\circ C$ | I_D | 2.5 | -3 | A |
| | $T_A=100^\circ C$ | | 1.6 | -1.9 | |
| | $T_C=25^\circ C$ | | 10 | -18 | |
| | $T_C=100^\circ C$ | | 6.3 | -12 | |
| Pulsed Drain Current ^A | | I_{DM} | 40 | -72 | A |
| Avalanche energy ^B | | EAS | 6.25 | 30.25 | mJ |
| Total Power Dissipation ^C | $T_A=25^\circ C$ | P_D | 2 | 2.5 | W |
| | $T_A=100^\circ C$ | | 0.8 | 1 | |
| | $T_C=25^\circ C$ | | 30 | 72 | |
| | $T_C=100^\circ C$ | | 12.5 | 29 | |
| Junction and Storage Temperature Range | | T_J, T_{STG} | -55~+150 | -55~+150 | $^\circ C$ |

Thermal resistance

| Parameter | | Symbol | NMOS | | PMOS | | Units |
|---|--------------|-----------------|------|-----|------|-----|--------------|
| | | | Typ | Max | Typ | Max | |
| Thermal Resistance Junction-to-Ambient ^D | Steady-State | $R_{\theta JA}$ | 50 | 60 | 40 | 50 | $^\circ C/W$ |
| Thermal Resistance Junction-to-Case | Steady-State | $R_{\theta JC}$ | 3.2 | 4 | 1.35 | 1.7 | |

Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|------------|----------------------|-------------------------|----------------------------|---------------|
| YJG10NP10A | F1 | YJG10NP10A | 5000 | 10000 | 100000 | 13" reel |



YJG10NP10A

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YJG10NP10B
FOR NEW DESIGN

■ NMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------------|---------------------|--|-----|-----|------|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | V _{GS} = 0V, I _D =250μA | 100 | - | - | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =100V, V _{GS} =0V | - | - | 1 | μA |
| | | V _{DS} =100V, V _{GS} =0V, T _J =150°C | - | - | 100 | |
| Gate-Body Leakage Current | I _{GSS} | V _{GS} = ±20V, V _{DS} =0V | - | - | ±100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D =250μA | 1.1 | 1.8 | 3 | V |
| Static Drain-Source On-Resistance | R _{DS(on)} | V _{GS} =10V, I _D =10A | - | 90 | 110 | mΩ |
| | | V _{GS} =4.5V, I _D =5A | - | 95 | 120 | |
| Diode Forward Voltage | V _{SD} | I _S =10A, V _{GS} =0V | - | 0.9 | 1.2 | V |
| Gate resistance | R _G | f=1MHz, Open drain | - | 1.6 | - | Ω |
| Maximum Body-Diode Continuous Current | I _S | | - | - | 10 | A |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C _{ISS} | V _{DS} =50V, V _{GS} =0V, f=1MHz | - | 900 | - | pF |
| Output Capacitance | C _{OSS} | | - | 35 | - | |
| Reverse Transfer Capacitance | C _{rss} | | - | 30 | - | |
| Switching Parameters | | | | | | |
| Total Gate Charge | Q _g | V _{GS} =10V, V _{DS} =50V, I _D =5A | - | 16 | - | nC |
| Gate-Source Charge | Q _{gs} | | - | 2.5 | - | |
| Gate-Drain Charge | Q _{gd} | | - | 2.6 | - | |
| Reverse Recovery Charge | Q _{rr} | I _F =5A, di/dt=350A/us | - | 90 | - | nC |
| Reverse Recovery Time | t _{rr} | | - | 35 | - | ns |
| Turn-on Delay Time | t _{D(on)} | V _{GS} =10V, V _{DD} =50V, I _D =5A R _{GEN} =2.2Ω | - | 5 | - | ns |
| Turn-on Rise Time | t _r | | - | 40 | - | |
| Turn-off Delay Time | t _{D(off)} | | - | 20 | - | |
| Turn-off fall Time | t _f | | - | 7 | - | |



YJG10NP10A

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PMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------------|---------------------|--|------|------|------|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | V _{GS} = 0V, I _D =-250μA | -100 | - | - | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =-100V, V _{GS} =0V | - | - | -1 | μA |
| | | V _{DS} =-100V, V _{GS} =0V, T _J =150°C | - | - | -100 | |
| Gate-Body Leakage Current | I _{GSS} | V _{GS} = ±20V, V _{DS} =0V | - | - | ±100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D =-250μA | -1 | -1.8 | -2.5 | V |
| Static Drain-Source On-Resistance | R _{DS(on)} | V _{GS} =-10V, I _D =-10A | - | 88 | 110 | mΩ |
| | | V _{GS} =-4.5V, I _D =-5A | - | 95 | 120 | |
| Diode Forward Voltage | V _{SD} | I _S =-10A, V _{GS} =0V | - | -0.9 | -1.3 | V |
| Gate resistance | R _G | f=1MHz, Open drain | - | 10 | - | Ω |
| Maximum Body-Diode Continuous Current | I _S | | - | - | -18 | A |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} =-50V, V _{GS} =0V, f=1MHz | - | 1050 | - | pF |
| Output Capacitance | C _{oss} | | - | 120 | - | |
| Reverse Transfer Capacitance | C _{rss} | | - | 25 | - | |
| Switching Parameters | | | | | | |
| Total Gate Charge | Q _g | V _{GS} =-10V, V _{DS} =-50V, I _D =-5A | - | 20 | - | nC |
| Gate-Source Charge | Q _{gs} | | - | 4 | - | |
| Gate-Drain Charge | Q _{gd} | | - | 4.5 | - | |
| Reverse Recovery Charge | Q _{rr} | I _F =-5A, di/dt=100A/us | - | 140 | - | nC |
| Reverse Recovery Time | t _{rr} | | - | 70 | - | ns |
| Turn-on Delay Time | t _{D(on)} | V _{GS} =-10V, V _{DD} =-50V, R _L =2.5Ω R _{GEN} =6Ω | - | 10 | - | ns |
| Turn-on Rise Time | t _r | | - | 30 | - | |
| Turn-off Delay Time | t _{D(off)} | | - | 77 | - | |
| Turn-off fall Time | t _f | | - | 81 | - | |

A. Repetitive rating; pulse width limited by max. junction temperature.

B. NMOS: T_J=25°C, V_{DD}=50V, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=5A.

PMOS: T_J=25°C, V_{DD}=-50V, V_G=-10V, R_G=25Ω, L=0.5mH, I_{AS}=-11A.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on the minimum recommend pad size, in the still air environment with T_A=25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



■ NMOS Typical Electrical and Thermal Characteristics Diagrams

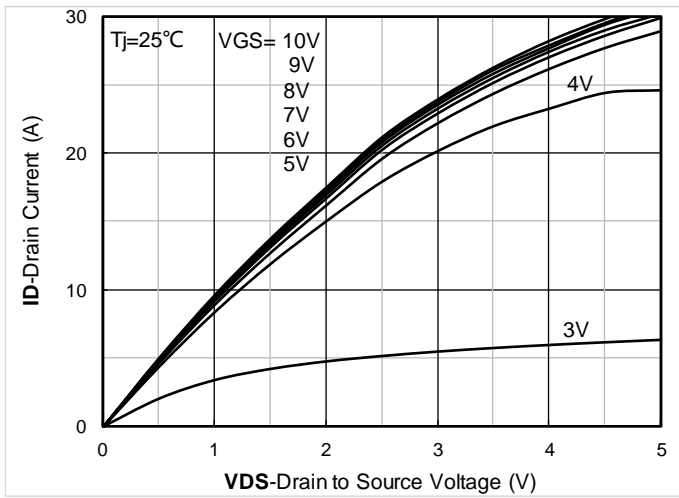


Figure1. Output Characteristics

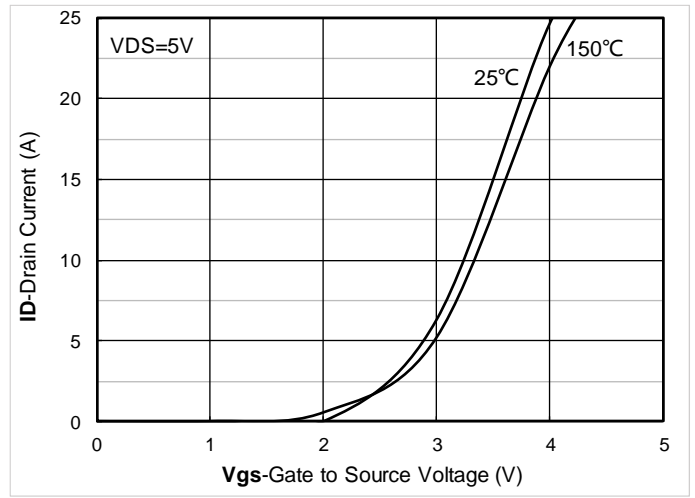


Figure2. Transfer Characteristics

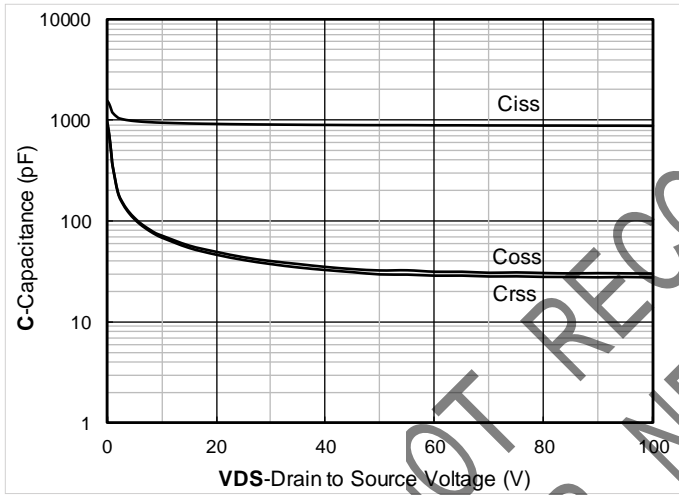


Figure3. Capacitance Characteristics

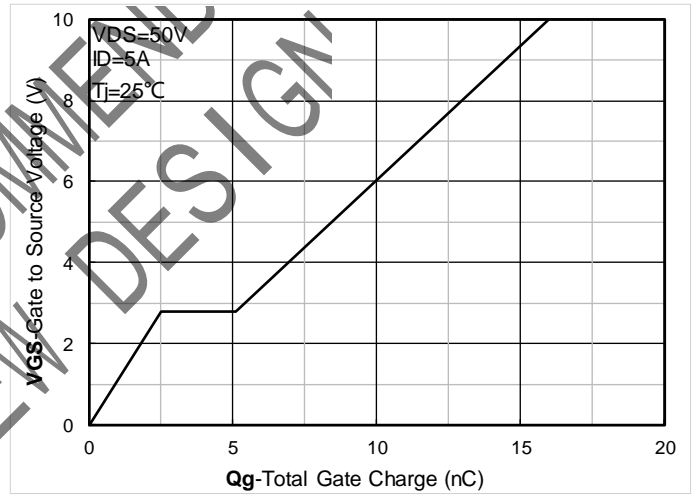


Figure4. Gate Charge

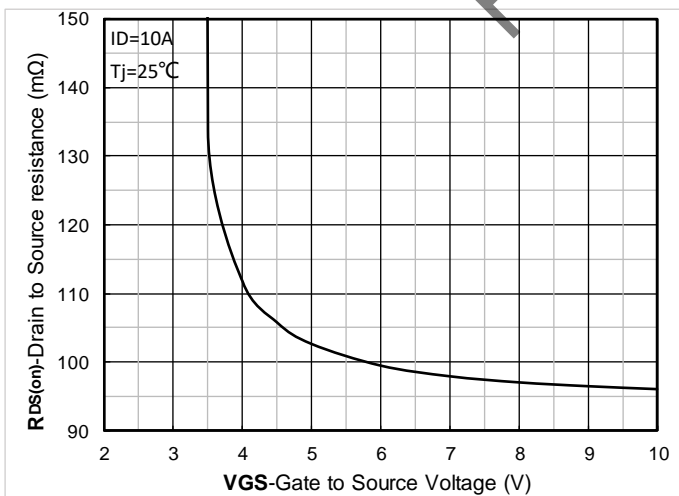


Figure5. On-Resistance vs Gate to Source Voltage

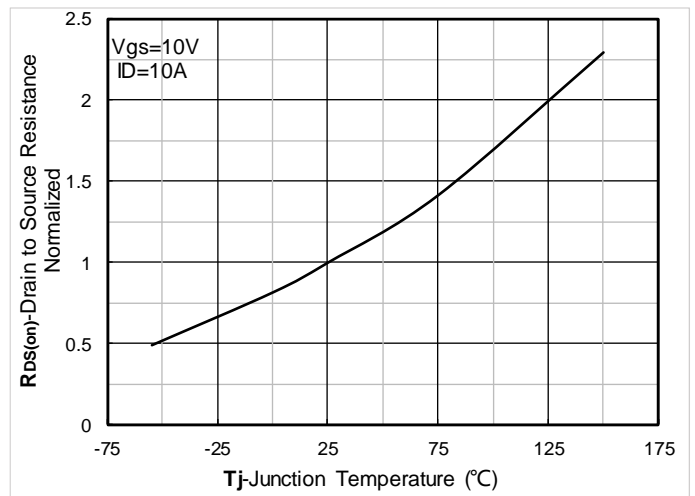


Figure6. Normalized On-Resistan

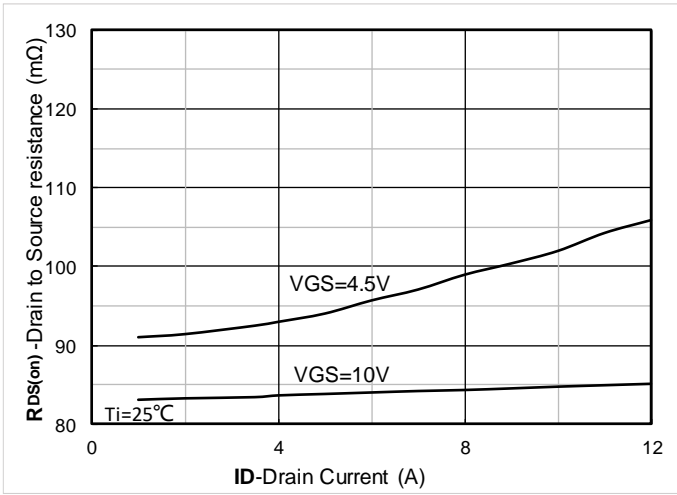


Figure7. RDS(on) VS Drain Current

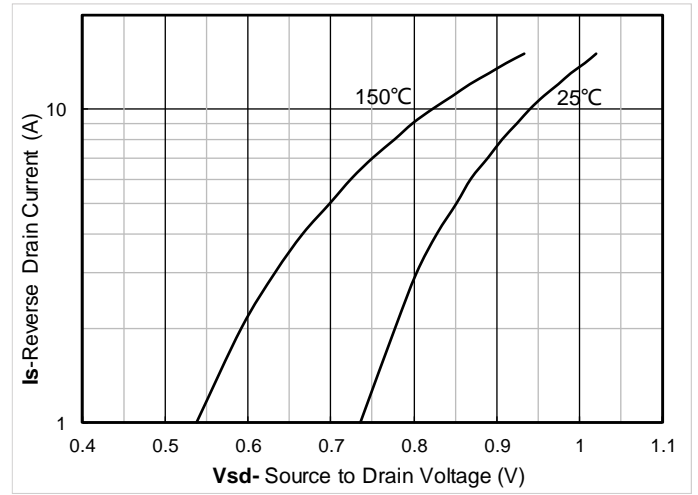


Figure8. Forward characteristics of reverse diode

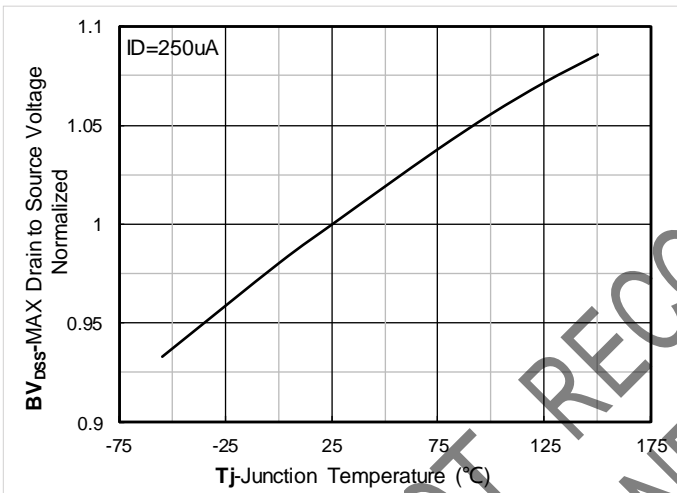


Figure9. Normalized breakdown voltage

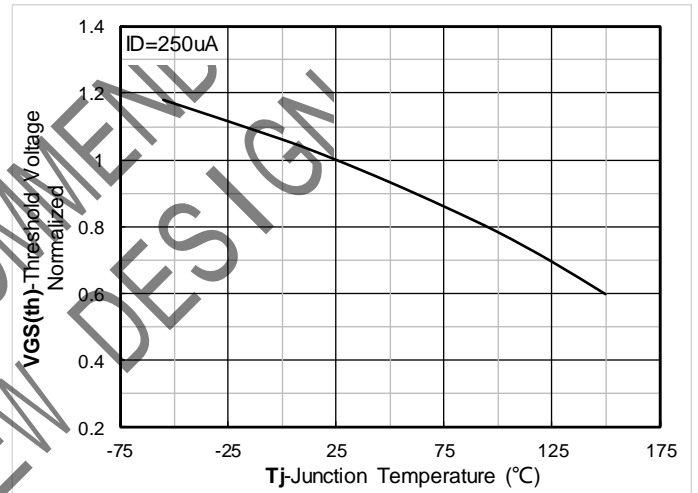


Figure10. Normalized Threshold voltage

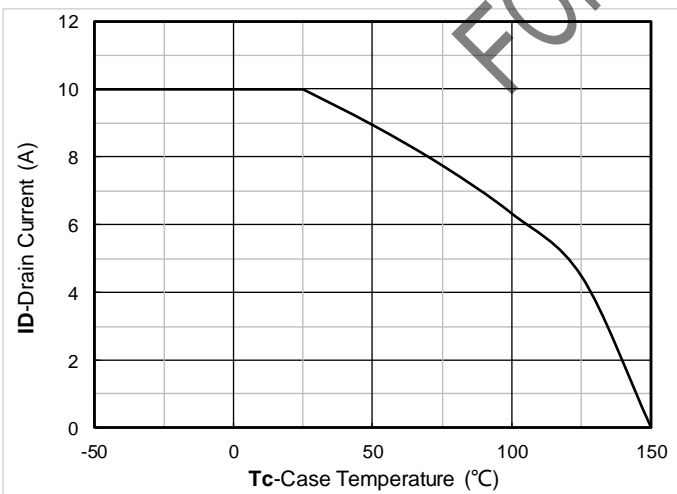


Figure11. Current dissipation

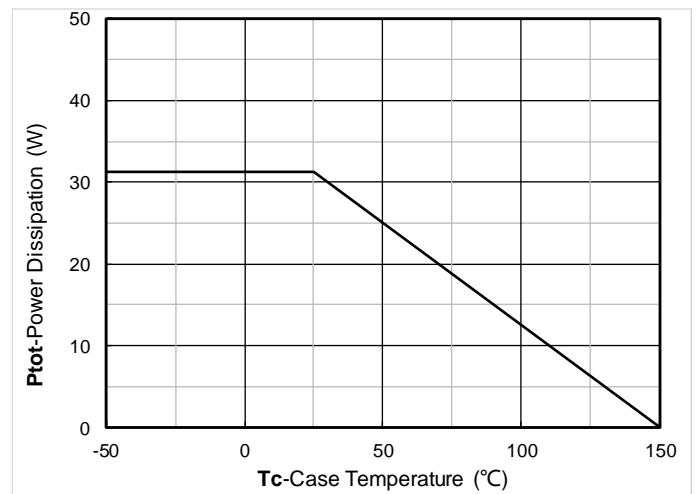


Figure12. Power dissipation

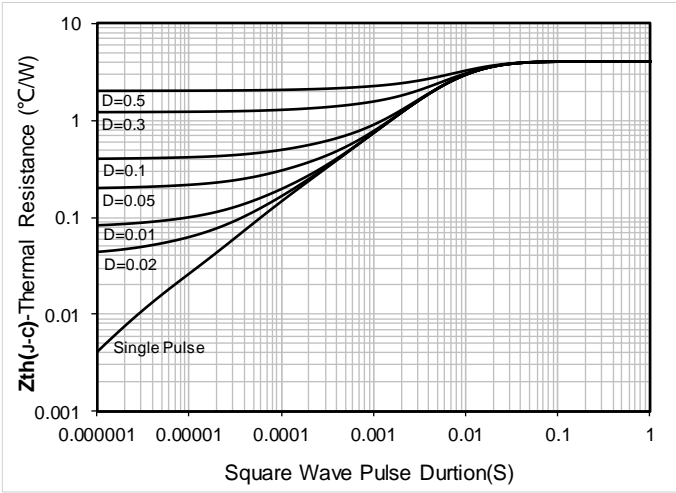


Figure13. Maximum Transient Thermal Impedance

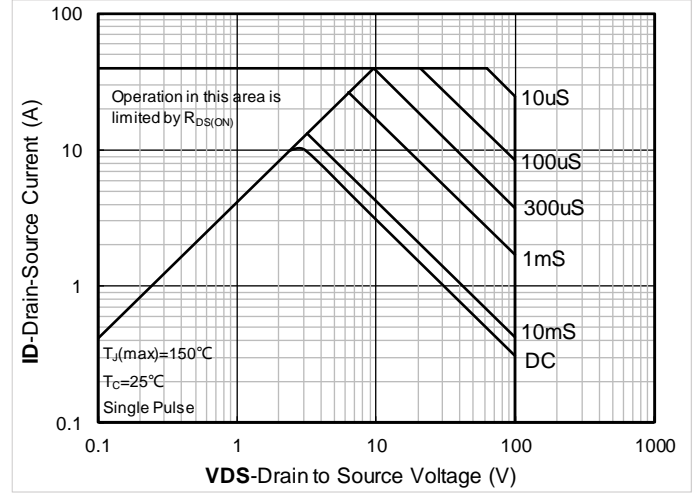


Figure14. Safe Operation Area

PMOS Typical Electrical and Thermal Characteristics Diagrams

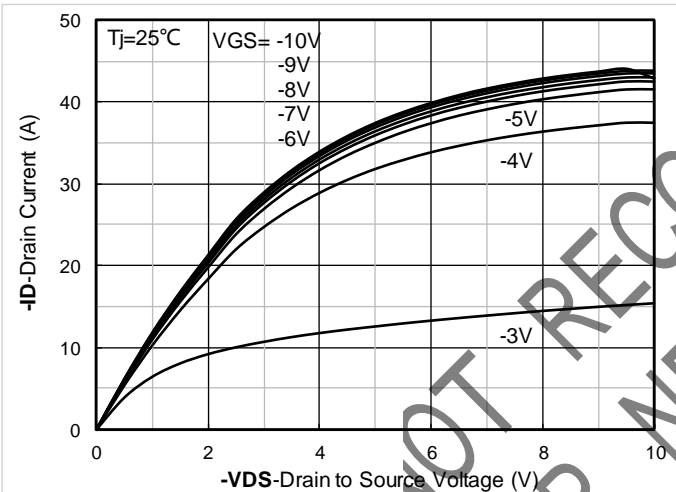


Figure1. Output Characteristics

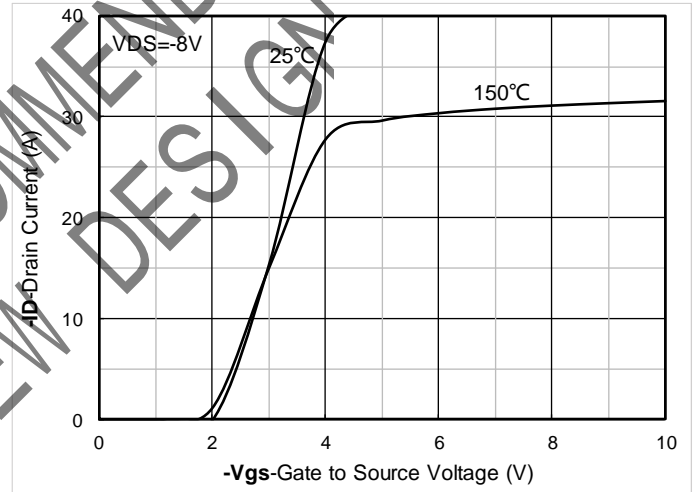


Figure2. Transfer Characteristics

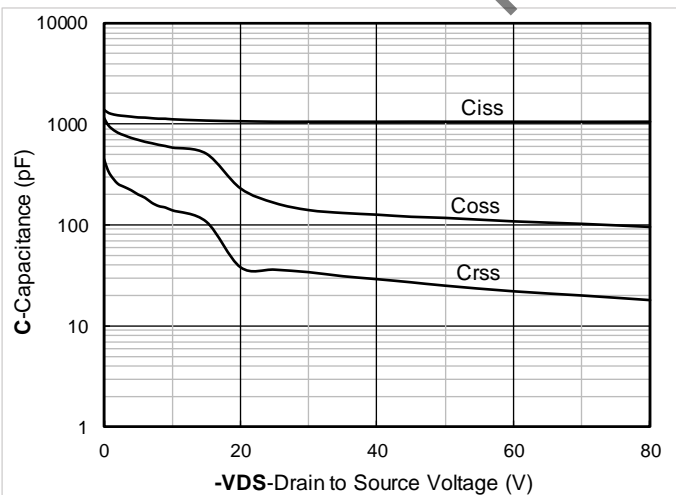


Figure3. Capacitance Characteristics

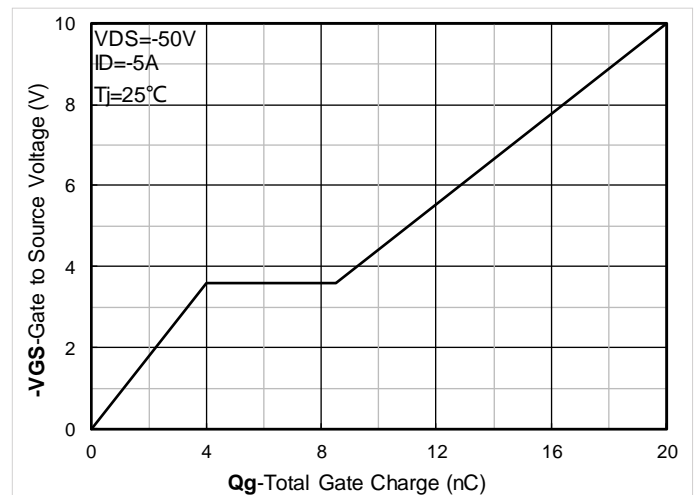


Figure4. Gate Charge



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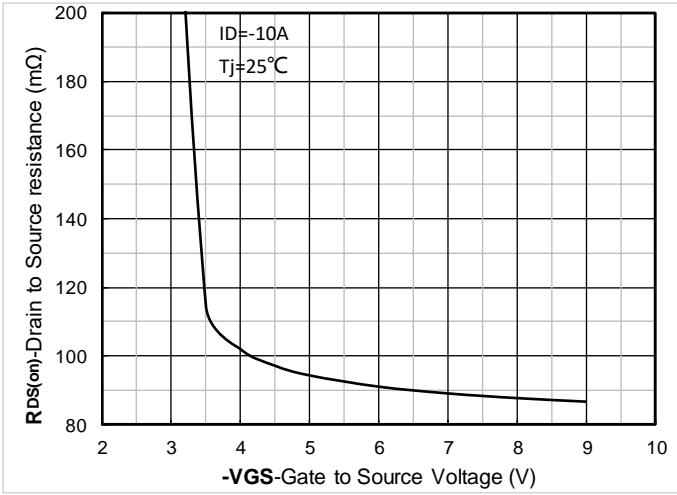


Figure5. On-Resistance vs Gate to Source Voltage

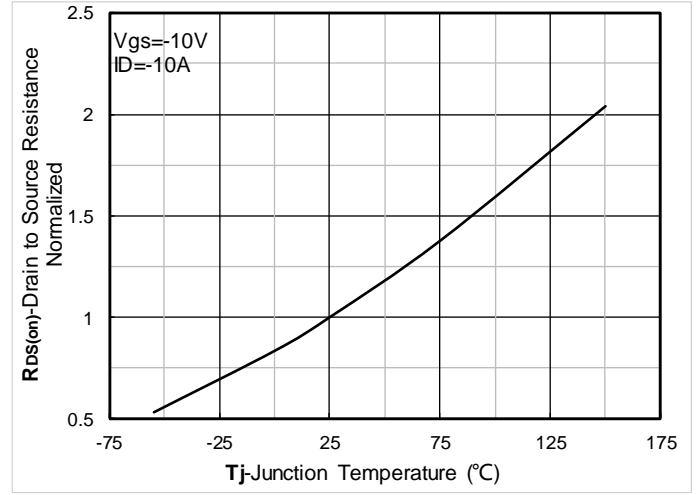


Figure6. Normalized On-Resistance

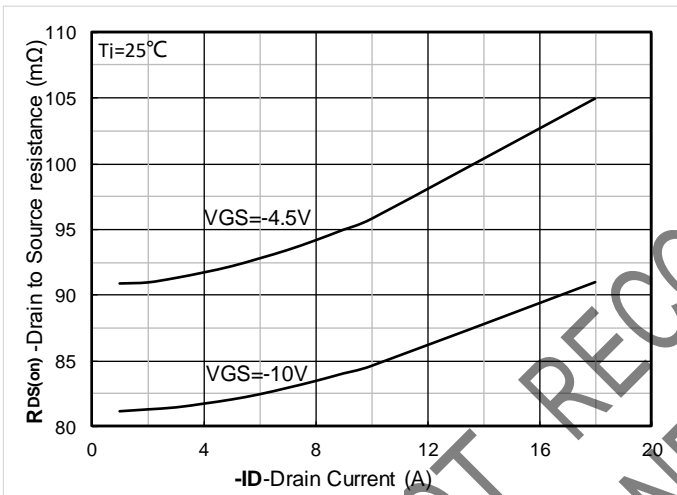


Figure7. RDS(on) VS Drain Current

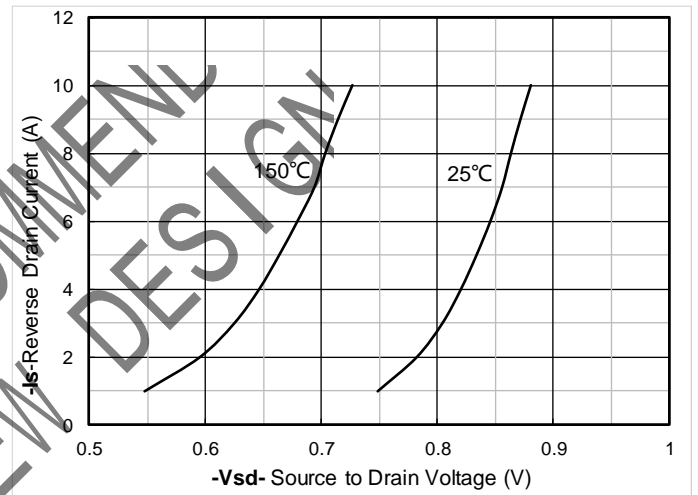


Figure8. Forward characteristics of reverse diode

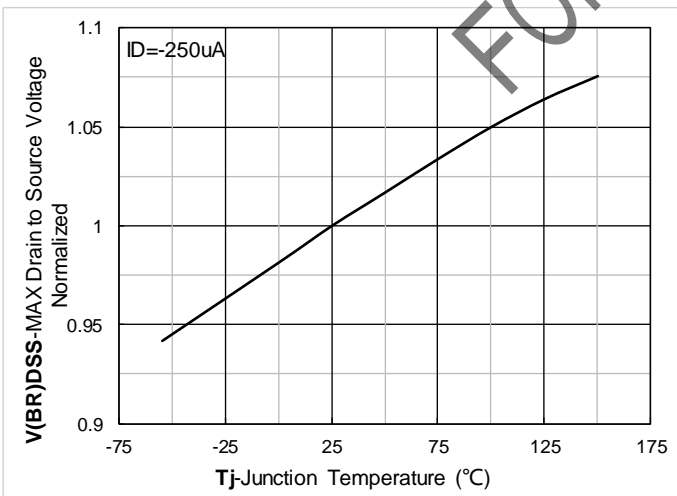


Figure9. Normalized breakdown voltage

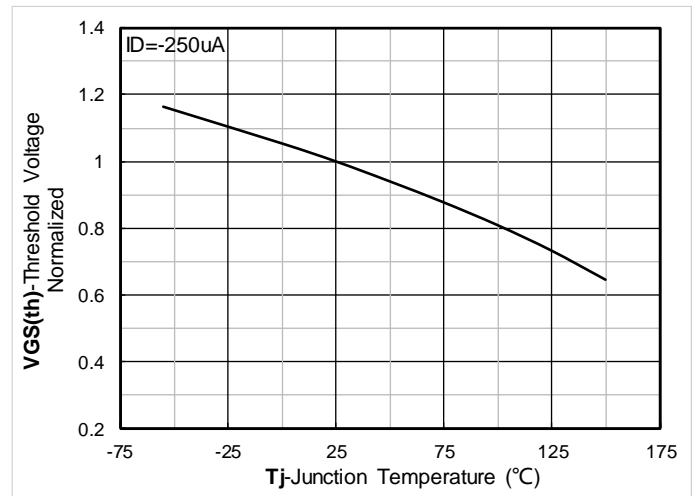


Figure10. Normalized Threshold voltage

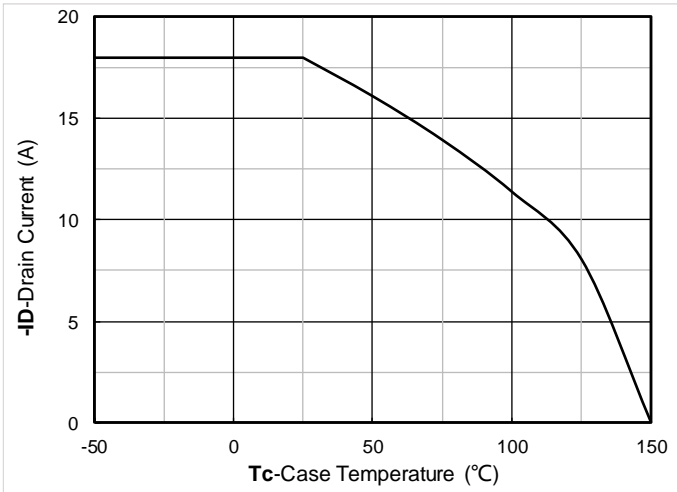


Figure11. Current dissipation

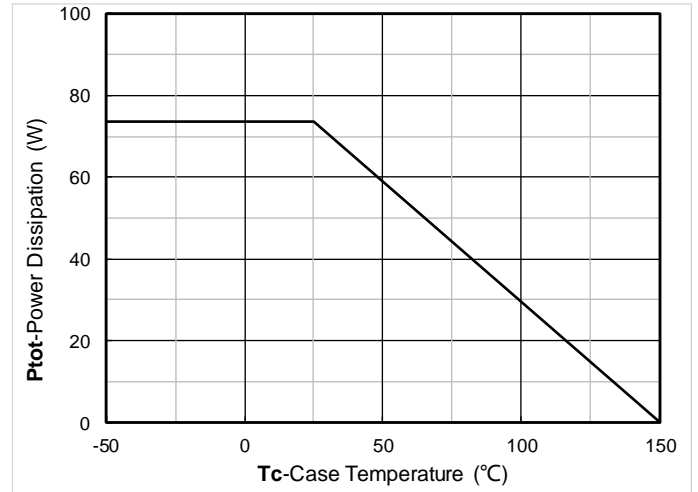


Figure12. Power dissipation

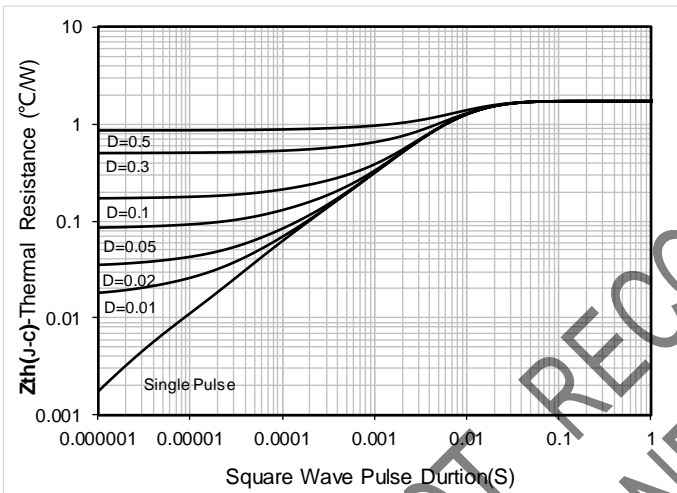


Figure13. Maximum Transient Thermal Impedance

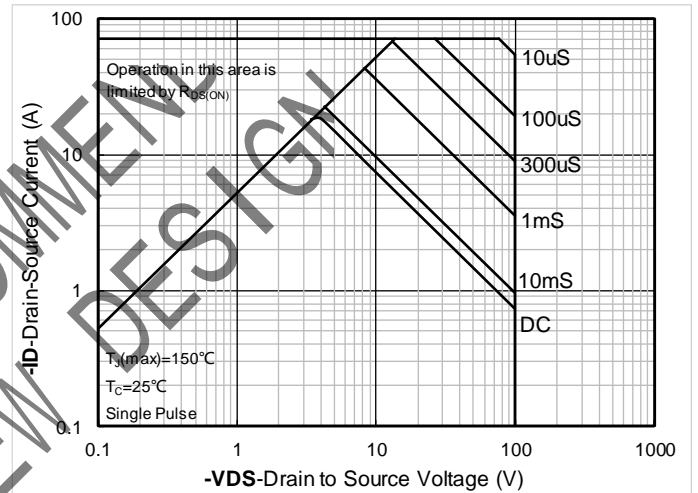


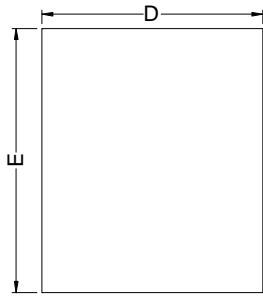
Figure14. Safe Operation Area



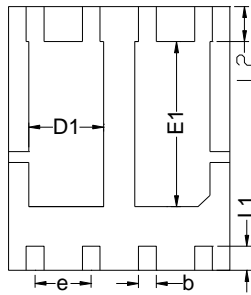
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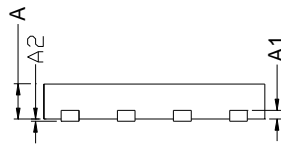
DFN5060-8L Package Information



Top View
正面视图

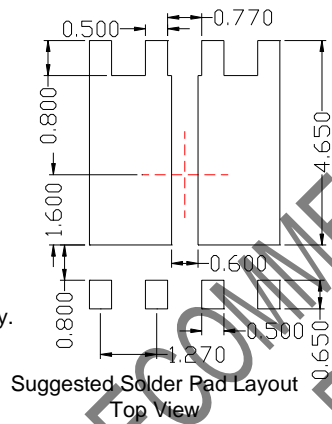


Bottom View
背面视图



Side View
侧面视图

| SYMBOL | MILLIMETER | | |
|--------|------------|------|------|
| | MIN | NOM | MAX |
| D | 4.90 | 5.00 | 5.10 |
| E | 5.90 | 6.00 | 6.10 |
| A | 0.70 | 0.80 | 0.90 |
| A1 | 0.20 BSC | | |
| A2 | | | 0.10 |
| D1 | 1.60 | 1.70 | 1.80 |
| E1 | 3.65 | 3.75 | 3.85 |
| L1 | 0.45 | 0.55 | 0.65 |
| L2 | 0.80 BSC | | |
| b | 0.30 | 0.40 | 0.50 |
| e | 1.27 BSC | | |



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

NOT RECOMMEND FOR NEW DESIGN



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